THAT WHICH IS CLAIMED IS:

1. An integrated circuit memory device, comprising:

a plurality of memory cells arranged as a plurality of blocks, each of the blocks including a plurality of primary memory cells that are coupled and decoupled to and from respective input/output lines responsive to a primary column select line and a plurality of redundant memory cells that are coupled and decoupled to and from respective ones of the input/output lines responsive to a redundant column select line;

a column select circuit, coupled to the primary column select lines and to the redundant column select lines, that drives a first primary column select line responsive to application of a first column address input and that drives a first redundant column select line in place of the first primary column select line responsive to application of a second column address input;

a plurality of sense amplifiers; and

an input/output control circuit configurable to selectively connect input/output lines to a sense amplifier such that a primary memory cell associated with the first primary column select line is coupled to the sense amplifier responsive to the first column address input and such that a redundant memory cell associated with the first redundant column select line is coupled to the sense amplifier responsive to the second column address input.

2. The device of Claim 1, wherein respective pluralities of input/output lines are associated with respective ones of the blocks of memory cells, wherein the first primary memory cell and the first redundant memory cell are in the same block of memory cells, and wherein the input/output control circuit couples the first primary memory cell and the first redundant memory cell to a sense amplifier via the plurality of input/output lines associated with the same block of memory cells.

3. The device of Claim 1, wherein respective pluralities of input/output lines are associated with respective ones of the blocks of memory cells, wherein the first primary memory cell and the first redundant memory cell are in respective first and second blocks of memory cells, and wherein the input/output control circuit couples the first primary memory cell and the first redundant memory cell to a sense amplifier via first and second input/output lines associated with respective ones of the first and second blocks of memory cells.

4. The memory device of Claim 1, wherein the input/output control circuit comprises:

a plurality of switches that couple and decouple the input/output lines to and from the plurality of sense amplifiers; and

a switch control circuit that controls the plurality of switches.

5. The memory device of Claim 4, wherein the switch control circuit is fuse programmable.

6. An integrated circuit memory device comprising:

a plurality of input/output blocks being divided into first and second blocks and having a first local input/output line and a first global input/output line for the first block, and a second local input/output line and a second global input/output line for the second block,

wherein data is input into and output from memory cells in the first block via the first local input/output line and the first global input/output line and data is input into and output from memory cells in the second block via the second local input/output line and the second global input/output line.

7. The integrated circuit memory device of Claim 6, wherein the first and second blocks each comprise column select lines for normal operation of primary memory cells and spare column select lines for replacing defective memory cells,

wherein a defective column select line in a first block of a predetermined input/output block is replaced with any one of a spare column select line in the first block of the predetermined input/output block, a spare column select line in a second block of the predetermined input/output block, and a spare column select line in a second block in an input/output block adjacent to the predetermined input/output block.

8. The integrated circuit memory device of Claim 7, wherein a defective column select line in the second block of the predetermined input/output block is replaced with any one of a spare column select line in the first block of the predetermined input/output block, a spare column select line in the second block of

the predetermined input/output block, and a spare column select line in a first block in another input/output block adjacent to the predetermined input/output block.

9. The integrated circuit memory device of Claim 7, wherein one of the column select lines and one of the spare column select lines are simultaneously activated by one column address in the adjacent input/output block if the defective column select line in the first block of the predetermined input/output block is replaced with a spare column select line in a second block of the adjacent input/output block.

10. The integrated circuit memory device of Claim 8, wherein one of the column select lines and one of the spare column select lines are simultaneously activated by one column address in the another adjacent input-output block if the defective column select line in the second block of the predetermined input/output block is replaced with a spare column select line in the first block of the another adjacent input/output block.

11. The integrated circuit memory device of Claim 7, further comprising:

a plurality of input/output sense amplifiers for each of the input/output blocks; and

a input/output control circuit connecting a second global input/output line in the adjacent input/output block to the input/output sense amplifier for the predetermined input/output block if the defective column select line in the first block of the predetermined input/output block is replaced with the spare column select line in the second block of the adjacent input/output block.

12. The integrated circuit memory device of Claim 11, wherein the input/output control circuit connects a first global input/output line of the predetermined input/output block to the input/output sense amplifier for the predetermined input/output block if the defective column select line in the first block of the predetermined input/output block is replaced with the spare column select line in the first block of the predetermined input/output block.

13. The integrated circuit memory device of Claim 12, wherein the input/output control circuit connects the second global input/output line of the predetermined input/output block to the input/output sense amplifier for the predetermined input/output block if the defective column select line in the first block of the predetermined input/output block is replaced with the spare column select line in the second block of the predetermined input/output block.

14. The integrated circuit memory device of Claim 13, wherein the input/output control circuit comprises:

a first switch for connecting the second global input/output line of the adjacent input/output block to the input/output sense amplifier for the predetermined input/output block in response to the activation of a first control signal;

a second switch for connecting the first global input/output line of the predetermined input/output block to the input/output sense amplifier for the predetermined input/output block in response to the activation of a second control signal;

a third switch for connecting the second global input/output line of the predetermined input/output block to the input/output sense amplifier for the predetermined input/output block in response to the activation of a third control signal; and

a control signal generator for generating the first, second, and third control signals,

wherein the first control signal is activated when the defective column select line in the first block of the predetermined input/output block is replaced with the spare column select line in the second block of the adjacent input/output block, the second control signal is activated when the defective column select line in the first block of the predetermined input/output block is replaced with the spare column select line in the first block of the predetermined input/output block, and the third control signal is activated when defective column select line in the first block of the predetermined input/output block is replaced with the spare column select line in the second block of the predetermined input/output block.

15. A integrated circuit memory device comprising:

a plurality of input/output blocks divided into first and second blocks, each having a plurality of memory cells, column select lines for normal operation of primary memory cells, and spare column select lines for replacing defective memory cells and each including a first local input/output line and a first global input/output line for the first block, and a second local input/output line and a second global input/output line for the second block,

wherein a defective column select line in a first block of a predetermined input/output block is replaced with any one of a spare column select line in the first block of the predetermined input/output block, a spare column select line in a second block of the predetermined input/output block, and a spare column select line in a second block of an input/output block adjacent to the predetermined input/output block.

16. The integrated circuit memory device of Claim 15, wherein a defective column select line in a second block of the predetermined input/output block is replaced with any one of a spare column select line in the first block of the predetermined input/output block, a spare column select line in the second block of the predetermined input/output block, and a spare column select line in a first block of another input/output block adjacent to the predetermined input/output block.

17. The integrated circuit memory device of Claim 15, wherein one of the column select lines and one of the spare column select lines are simultaneously activated by one column address in an adjacent input/output block if the defective column select line in the first block of the predetermined input/output block is replaced with the spare column select line in the second block of the adjacent input/output block.

18. The integrated circuit memory device of Claim 16, wherein one of the column select lines and one of the spare column select lines are simultaneously activated by one column address in the adjacent input/output block if the defective column select line in the second block of the predetermined input/output block is replaced with the spare column select line in the first block of the adjacent input/output block.

19. The integrated circuit memory device of Claim 15, further comprising:

a plurality of input/output sense amplifiers for each of the input/output blocks; and

a switch controller for connecting a second global input/output line of an adjacent input/output to an input/output sense amplifier for the predetermined input/output block if the defective column select line in the first block of the predetermined input/output block is replaced with the spare column select line in the second block of the adjacent input/output block.

20. The integrated circuit memory device of Claim 19, wherein the input/output control circuit connects a first global input/output line of the predetermined input/output block to the input/output sense amplifier for the predetermined input/output block if the defective column select line in the first block of the predetermined input/output block is replaced with the spare column select line in the first block of the predetermined input/output block.

21. The integrated circuit memory device of Claim 20, wherein the input/output control circuit connects the second global input/output line of the predetermined input/output block to the input/output sense amplifier for the predetermined input/output block if the defective column select line in the first block of the predetermined input/output block is replaced with the spare column select line in the second block of the predetermined input/output block.

22. The integrated circuit memory device of Claim 21, wherein the input/output control circuit comprises:

a first switch for connecting the second global input/output line of the adjacent input/output block to the input/output sense amplifier for the predetermined input/output block in response to the activation of a first control signal;

a second switch for connecting the first global input/output line of the predetermined input/output block to the input/output sense amplifier for the predetermined input/output block in response to the activation of a second control signal;

a third switch for connecting the second global input/output line of the predetermined input/output block to the input/output sense amplifier for the

predetermined input/output block in response to the activation of a third control signal; and

a control signal generator for generating the first, second, and third control signals,

wherein the first control signal is activated when the defective column select line in the first block of the predetermined input/output block is replaced with the spare column select line in the second block of the adjacent input/output block, the second control signal is activated when the defective column select line in the first block of the predetermined input/output block is replaced with the spare column select line in the first block of the predetermined input/output block, and the third control signal is activated when the defective column select line in the first block of the predetermined input/output block is replaced with the spare column select line in the second block of the predetermined input/output block.

23. A method of operating a memory device that includes a plurality of memory cells arranged as a plurality of blocks, each of the blocks including a plurality of primary memory cells that are coupled and decoupled to and from respective input/output lines responsive to a primary column select line and a plurality of redundant memory cells that are coupled and decoupled to and from respective ones of the input/output lines responsive to a redundant column select line, the method comprising:

driving a first primary column select line responsive to application of a first column address input;

driving a first redundant column select line in place of the first primary column select line responsive to application of a second column address input; and

selectively connecting input/output lines to a sense amplifier such that a primary memory cell associated with the first primary column select line is coupled to the sense amplifier responsive to the first column address input and such that a redundant memory cell associated with the first redundant column select line is coupled to the sense amplifier responsive to the second column address input.

24. The method of Claim 23, wherein respective pluralities of input/output lines are associated with respective ones of the blocks of memory cells, wherein the first primary memory cell and the first redundant memory cell are in the same block

of memory cells, and wherein selectively connecting input/output lines to a sense amplifier comprises coupling the first primary memory cell and the first redundant memory cell to the sense amplifier via the plurality of input/output lines associated with the same block of memory cells.

25. The method of Claim 23, wherein respective pluralities of input/output lines are associated with respective ones of the blocks of memory cells, wherein the first primary memory cell and the first redundant memory cell are in respective first and second blocks of memory cells, and wherein selectively connecting input/output lines to a sense amplifier comprises coupling the first primary memory cell and the first redundant memory cell to a sense amplifier via first and second input/output lines associated with respective ones of the first and second blocks of memory cells.

26. The method of Claim 23, wherein selectively connecting input/output lines to a sense amplifier comprises operating a plurality of switches that couple and decouple the input/output lines to and from the plurality of sense amplifiers, and wherein selectively connecting input/output lines to a sense amplifier is preceded by programming a switch control circuit to operate the plurality of switches such that a primary memory cell associated with the first primary column select line is coupled to the sense amplifier responsive to the first column address input and such that a redundant memory cell associated with the first redundant column select line is coupled to the sense amplifier responsive to the second column address input.